WHAT IS CLAIMED IS:

1. A system for frequency and phase correction in a phase-locked loop (PLL), the system comprising:

a phase frequency detector operable to:

detect a frequency difference and a phase difference between a clock signal and a comparison signal, the comparison signal being derived from an output signal of the PLL;

communicate the frequency difference to a first charge pump generating a first current; and

communicate the phase difference to a second charge pump generating a voltage ;

the first charge pump operable to:

modify the first current according to the frequency difference; and

communicate the first current to the current summer;

the second charge pump operable to:

modify the voltage according to the phase difference; and

communicate the voltage to a voltage-to-current (V2I) converter;

the V2I converter operable to:

generate a second current corresponding to the voltage; and

communicate the second current to the current summer;

the current summer operable to:

combine the first and second currents with each other to generate a control current for a current-controlled oscillator (CCO); and

communicate the control current to the CCO; and

the CCO operable to generate one or more oscillating signals according to the first and second currents, a frequency of an oscillating signal from the CCO changing in response to the modification of the first current, a phase of the oscillating signal changing in response to the modification of the second current.

2. The system of Claim 1, wherein the CCO comprises one or more transistor devices for clock dithering.

3. The system of Claim 1, wherein the current summer comprises a current addition and subtraction circuit for clock dithering.

4. The system of Claim 1, wherein the first and second charge pumps and V2I converter collectively function as a proportional integral (PI) circuit.

5. The system of Claim 1, wherein each of the oscillating signals has a frequency and a phase, the frequencies of the oscillating signals being at least approximately equal to each other, the phases of the oscillating signal being at least approximately evenly spaced about 360°.

6. The system of Claim 1, wherein:

the oscillating signals from the CCO are sinusoidal; and

the system further comprises one or more converters that are each operable to covert one or more oscillating signals from the CCO into substantially square waves.

7. The system of Claim 1, wherein the CCO comprises one or more CCO elements that are each operable to generate two oscillating signals that are at least approximately 180° apart from each other in phase.

8. A method for frequency and phase correction in a phase-locked loop (PLL), the method comprising:

using a phase frequency detector to:

detect a frequency difference and a phase difference between a clock signal and a comparison signal, the comparison signal being derived from an output signal of the PLL;

communicate the frequency difference to a first charge pump generating a first current; and

communicate the phase difference to a second charge pump generating a voltage;

using the first charge pump to:

modify the first current according to the frequency difference; and

communicate the first current to a current summer;

using the second charge pump operable to:

modify the voltage according to the phase difference; and

communicate the voltage to a voltage-to-current (V2I) converter;

using the V2I converter to:

generate a second current corresponding to the voltage; and

communicate the second current to the current summer;

using the current summer to:

combine the first and second currents with each other to generate a control current for a current-controlled oscillator (CCO); and

communicate the control current to the CCO; and

using the CCO to generate one or more oscillating signals according to the first and second currents, a frequency of an oscillating signal from the CCO changing in response to the modification of the first current, a phase of the oscillating signal changing in response to the modification of the second current.

9. The method of Claim 8, wherein the CCO comprises one or more transistor devices for clock dithering.

10. The method of Claim 8, wherein the current summer comprises a current addition and subtraction circuit for clock dithering.

11. The method of Claim 8, wherein the first and second charge pumps and V2I converter collectively function as a proportional integral (PI) circuit.

12. The method of Claim 8, wherein each of the oscillating signals has a frequency and a phase, the frequencies of the oscillating signals being at least approximately equal to each other, the phases of the oscillating signal being at least approximately evenly spaced about 360°.

13. The method of Claim 8, wherein:

the oscillating signals from the CCO are sinusoidal; and

the system further comprises one or more converters that are each operable to covert one or more oscillating signals from the CCO into substantially square waves.

14. The method of Claim 8, wherein the CCO comprises one or more CCO elements that are each operable to generate two oscillating signals that are at least approximately 180° apart from each other in phase.

15. Logic for frequency and phase correction in a phase-locked loop (PLL), the logic encoded in media and when executed providing:

a phase frequency detector operable to:

detect a frequency difference and a phase difference between a clock signal and a comparison signal, the comparison signal being derived from an output signal of the PLL;

communicate the frequency difference to a first charge pump generating a first current; and

communicate the phase difference to a second charge pump generating a voltage ;

the first charge pump operable to:

modify the first current according to the frequency difference; and

communicate the first current to the current summer;

the second charge pump operable to:

modify the voltage according to the phase difference; and

communicate the voltage to a voltage-to-current (V2I) converter;

the V2I converter operable to:

generate a second current corresponding to the voltage; and

communicate the second current to the current summer;

the current summer operable to:

combine the first and second currents with each other to generate a control current for a current-controlled oscillator (CCO); and

communicate the control current to the CCO; and

the CCO operable to generate one or more oscillating signals according to the first and second currents, a frequency of an oscillating signal from the CCO changing in response to the modification of the first current, a phase of the oscillating signal changing in response to the modification of the second current.

16. The logic of Claim 15, wherein the CCO comprises one or more transistor devices for clock dithering.

17. The logic of Claim 15, wherein the current summer comprises a current addition and subtraction circuit for clock dithering.

18. The logic of Claim 15, wherein the first and second charge pumps and V2I converter collectively function as a proportional integral (PI) circuit.

19. The logic of Claim 15, wherein each of the oscillating signals has a frequency and a phase, the frequencies of the oscillating signals being at least approximately equal to each other, the phases of the oscillating signal being at least approximately evenly spaced about 360°.

20. The logic of Claim 15, wherein:

the oscillating signals from the CCO are sinusoidal; and

the system further comprises one or more converters that are each operable to covert one or more oscillating signals from the CCO into substantially square waves.

21. The logic of Claim 15, wherein the CCO comprises one or more CCO elements that are each operable to generate two oscillating signals that are at least approximately 180° apart from each other in phase.